



ER3400 ER3401

4096 Bit High Speed Electrically Alterable Read Only Memories

FEATURES

- 1024 x 4 Organization, Fully Decoded
- Single Word or Block Electrically Erasable
- TTL Compatible with Resistor Pull-Ups
- Three State Output
- ER3400: 650ns Access Time
- ER3401: 950ns Access Time
- 7.8 us Cycle Time
- 10 ms Word or Block Erase Time
- 1 ns Write Time
- 22 Pin DIP
- P-Channel Metal Gate MNOS Technology
- 0°C to 70°C Operation
- +5, -12, -30V Power Supplies
- 10⁶ Erase-Write Cycles per Word
- 2 x 10¹¹ Read Cycles per Word
- 10 Year Unpowered Data Storage — 10 Years

DESCRIPTION

The ER3400 and ER3401 are word alterable ROMs intended for use as read-mostly memories. Each operates with one clock, **CHIPENABLE (CE)**, which also serves for chip selection. All other pins of each device can be paralleled with other EAROMs. Any one of four possible operating modes can be selected by setting the proper binary code on the C0-C1 control lines and pulsing the device with **CE**. The four modes are Read, Write, Word Erase and Block Erase. The ER3400/3401 will sense the control lines and change modes only when pulsed by **CE**. When in the Read mode, data is read during each **CE** pulse. Writing or erasing of a word continues for as long as the device is in the Write or Erase mode. Each write or erase word cycle must be ended by a dummy read operation.

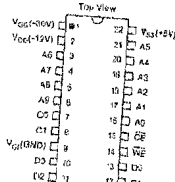
A **WRITE ENABLE (WE)** input pulse indicates to the ER3400/3401 that the data on the D0-D3 data input/output lines is valid input data. This data is then stored internally for use during the write operation.

PIN FUNCTIONS

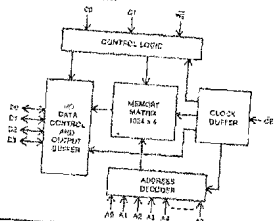
A ₀ -A ₉	10-Bit Word Address															
D ₀ -D ₃	Data input and output pins															
CE	Chip Enable, Chip selected when $\overline{\text{CE}}$ is pulsed to logic "0".															
C ₀ , C ₁	Mode Control Inputs															
	<table><tr><th>C₀</th><th>C₁</th><th>Mode</th></tr><tr><td>0</td><td>1</td><td>Block Erase Mode: erase operation performed on all words</td></tr><tr><td>1</td><td>1</td><td>Word Erase Mode: stored data is erased at addressed location.</td></tr><tr><td>0</td><td>0</td><td>Read Mode: addressed data read after leading edge of $\overline{\text{CE}}$ pulse</td></tr><tr><td>1</td><td>0</td><td>Write Mode: input data written at addressed location.</td></tr></table>	C ₀	C ₁	Mode	0	1	Block Erase Mode: erase operation performed on all words	1	1	Word Erase Mode: stored data is erased at addressed location.	0	0	Read Mode: addressed data read after leading edge of $\overline{\text{CE}}$ pulse	1	0	Write Mode: input data written at addressed location.
C ₀	C ₁	Mode														
0	1	Block Erase Mode: erase operation performed on all words														
1	1	Word Erase Mode: stored data is erased at addressed location.														
0	0	Read Mode: addressed data read after leading edge of $\overline{\text{CE}}$ pulse														
1	0	Write Mode: input data written at addressed location.														
WE	Write Enable: input data read when $\overline{\text{WE}}$ is pulsed to logic "0".															
V _{SS}	Substrate supply. Normally at +5 volts.															
V _{SI}	Ground Input															
V _{DD}	Power Supply Input. Normally at -12 volts															
V _{GG}	Power Supply Input. Normally at -30 volts															

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



No particular order of power supply sequencing on or off is required for the ER3400. Circuits are provided to force the device into the read mode during power turn on. Erasing and writing are inhibited if V_{DD} or V_{GG} are not at proper operating levels. For the ER3401, V_{Q1} must be turned on after V_{DD} is stable and removed before V_{DD} is turned off.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) -40V to +0.3V
 Storage temperature (with data retention) -40°C to +70°C
 Storage temperature (without data retention) -65°C to +150°C
 Soldering temperature of leads (10 seconds) +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{SS} = +5V ±5%
 V_{DD} = -12V ±5%
 V_{Q1} = -30V ±5%
 V_{Q1} = GND
 Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "1"	V _{IH}	V _{SS} -1.5	—	V _{SS} +0.3	Volts	
Input Logic "0"	V _{IL}	-10	—	0.8	Volts	
Output Logic "1"	V _{OH}	V _{SS} -1.5	—	—	Volts	I _{OH} = -2mA
Output Logic "0"	V _{OL}	—	—	0.4	Volts	I _{OL} = 2mA
Control Input Leakage	I _{IC}	—	—	-2.0	µA	V _{IN} = V _{SS} -15 Volts
Data Input Leakage	I _{LC}	—	—	-10.0	µA	V _{IN} = V _{SS} -15 Volts
Power Supply Current						
V _{DD} Supply Current: Chip selected	I _{DD}	—	—	-25.0	mA	V _{DD} = V _{SS} -17 Volts
Chip de-selected	I _{DD}	—	—	-7.0	mA	V _{DD} = V _{SS} -17 Volts
V _{Q1} Supply Current	I _{Q1}	—	—	-3.0	mA	V _{Q1} = V _{SS} -35 Volts
V _{SS} Supply Current: Chip selected	I _{SS}	—	—	-25.0	mA	V _{DD} = V _{SS} -17V, V _{Q1} = V _{SS} -35V
Chip de-selected	I _{SS}	—	—	-11.5	mA	V _{DD} = V _{SS} -17V, V _{Q1} = V _{SS} -35V
AC CHARACTERISTICS						
Input capacitance - control inputs	C _I	—	8	8	pf	
Input capacitance - data inputs	C _D	—	8	10	pf	
Read Mode Characteristics						
Address and control to CE	t _{D1}	0	—	—	ns	
Address and control hold time	t _{D2}	250	—	—	ns	
CE to Data I/O Off	t _{D3}	50	—	200	ns	
CE high	t _{D4}	900	—	—	ns	
Access time: ER3400	t _A	—	—	650	ns	RL = 2K to V _{SS} , CL = 100pf
ER3401	t _A	—	—	950	ns	
CE pulse width: ER3400	t _{CE}	950	—	100000	ns	
ER3401	t _{CE}	950	—	100000	ns	
Read cycle time	t _{CY}	1350 + t _r + t _f	—	—	ns	
CE rise, fall time	t _r , t _f	0	—	100	ns	
Write/Erase Mode Characteristics						
Address and control to CE	t _{D11}	0	—	—	ns	
Address and control hold time	t _{D12}	250	—	—	ns	
CE fall to WE fall delay	t _{D13}	0	—	—	ns	
WE rise to CE rise delay	t _{D14}	-50	—	—	ns	
Data stable to WE	t _{D15}	0	—	—	ns	
WE rise to End of Data Stable	t _{D16}	50	—	—	ns	
CE pulse width: ER3400	t _{CE}	650	—	100000	ns	{ WE rise may overlap CE rise by a maximum of 50ns
ER3401	t _{CE}	950	—	100000	ns	
WE pulse width	t _{WE}	400	—	—	ns	
Write time	t _W	1	—	2	ms	
Erase time	t _E	10	—	—	ms	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

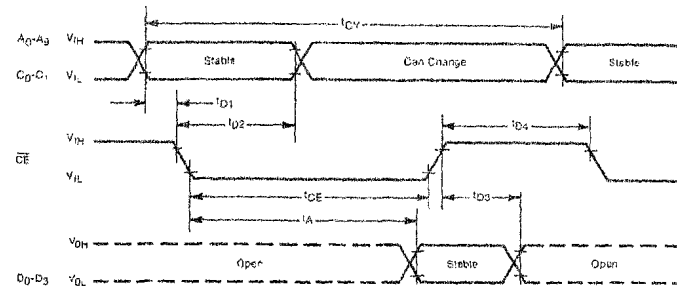


Fig.1: READ MODE TIMING

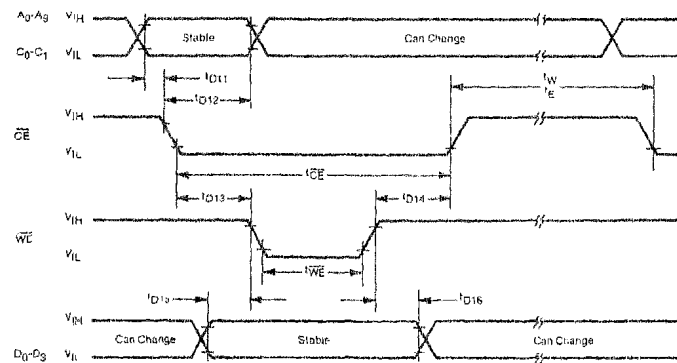


Fig.2: WRITE AND ERASE MODE TIMING

TYPICAL CHARACTERISTIC CURVES

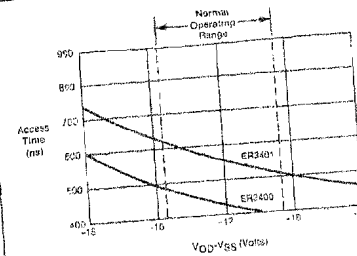


Fig.3: TYPICAL ACCESS TIME vs. POWER SUPPLY VOLTAGE @ 25°C

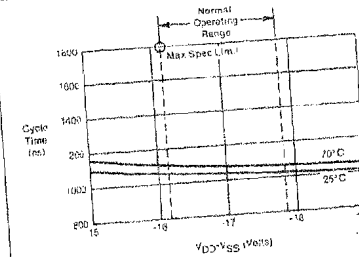


Fig.4: TYPICAL CYCLE TIME vs. POWER SUPPLY VOLTAGE

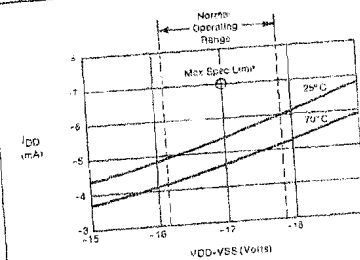


Fig.5: I_{DD} vs. $V_{DD}-V_{SS}$ POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

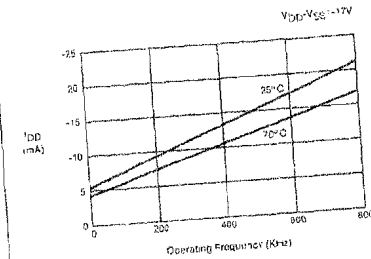


Fig.6: I_{DD} vs. OPERATING FREQUENCY IN READ MODE AND SELECTED

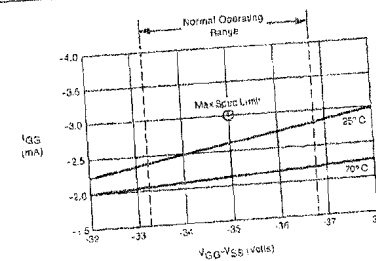


Fig.7: I_{GG} vs. $V_{GG}-V_{SS}$ POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED